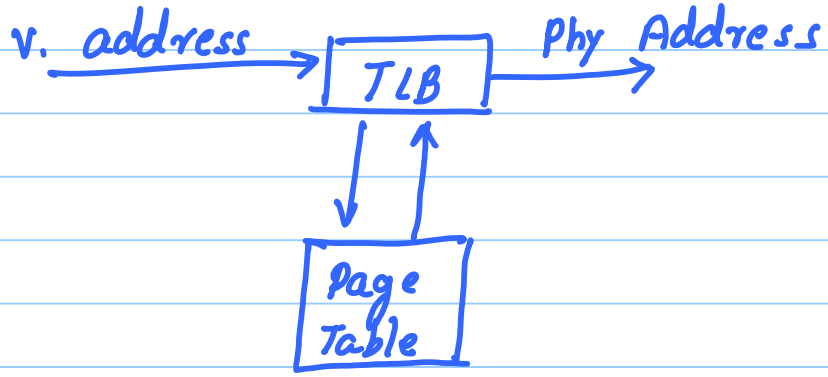
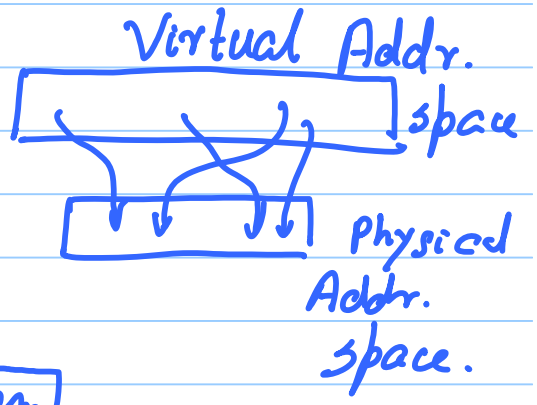
Oct 18th.

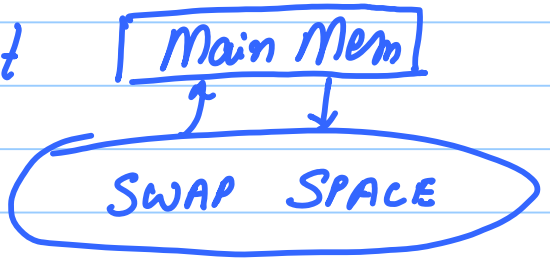
Note Title 18-10-2011





1) TLB Entry Replacement

2) Page replacement



REPLACEMENT POLICY

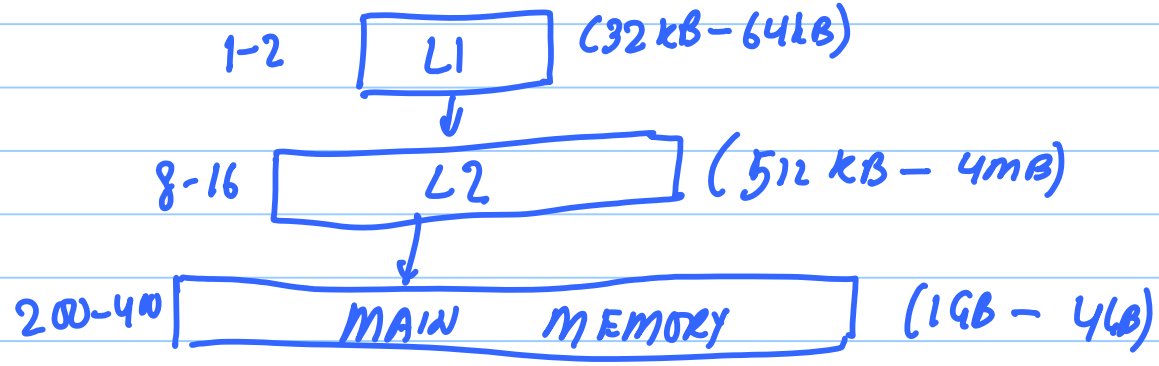
1) FIFO

2) LRU (Least Recently Used)

Caches.

What happens after translation?

Hierarchy in the physical Address space



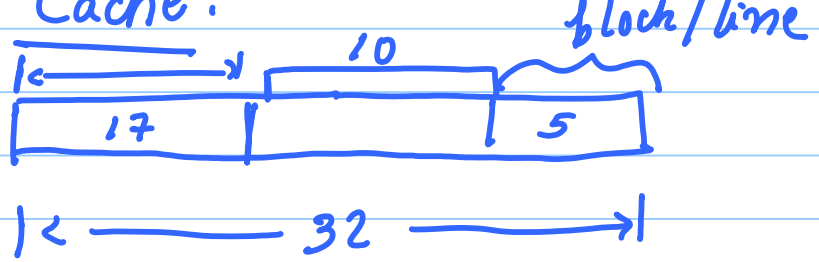
Structure of a cache

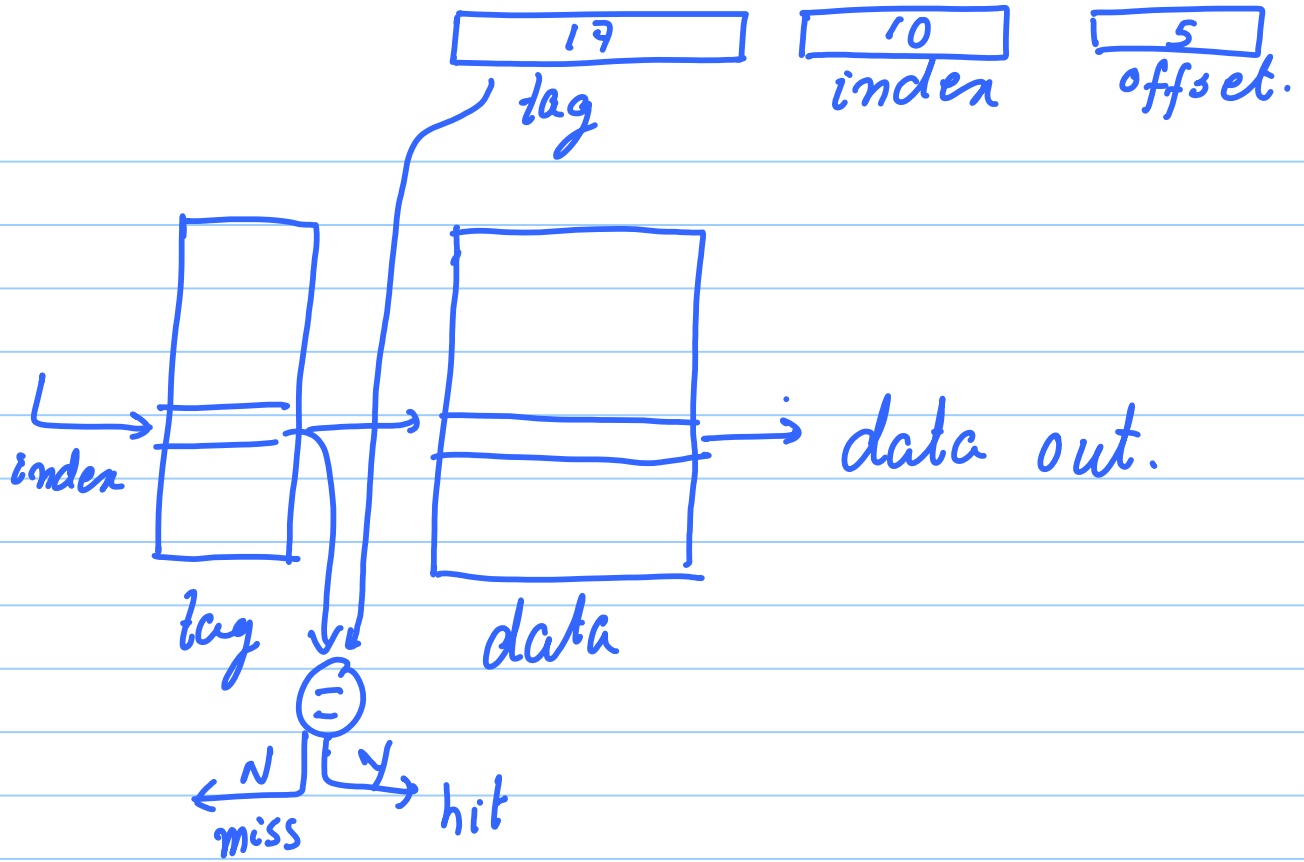
MEMORY ADDRESS: 32 bits.

Block size : 32 bytes

(8 integers in one block)

Direct Mapped Cache:




17
tag
10
index
5
offset.
index
data out.
tag
data
=
N
miss
Y
hit

Fully Associative Cache